WHAT IS CLAIMED IS:

1. A microcomputer comprising:

a nonvolatile memory including at least a first storage area and a second storage area in which delete and write of data is electrically performed independently, wherein

a plurality of interrupt vectors indicating respective storage places of a plurality of interrupt programs executed upon requesting of an interrupt is stored in the first storage area, and

a plurality of alternate interrupt vectors corresponding to the respective interrupt vectors is stored in the second storage area;

a central processing unit that has a mechanism to access the nonvolatile memory;

a flag indicating that the first storage area is not accessible; and

a conversion circuit that, based on a state of the flag, converts an address indicating a storage place of the interrupt vector that is accessed by the central processing unit into an address indicating a storage place of the corresponding alternate interrupt vector.

2. The microcomputer according to claim 1, wherein the conversion circuit includes a plurality of registers to which addresses indicating the respective storage places of the alternate interrupt vectors are set, and outputs an address that is set in the register corresponding to the interrupt vector address accessed by the central processing unit.

3. The microcomputer according to claim 1, wherein

the conversion circuit includes a register to which an offset quantity of the address indicating a storage place of the alternate interrupt vector corresponding to the address indicating the storage place of the interrupt vector is set, and

a value obtained by adding the offset quantity set in the register to the interrupt vector address accessed by the central processing unit is output from the conversion circuit.

4. The microcomputer according to claim 1, wherein the conversion circuit comprises hardware that performs a predetermined conversion operation.

5. The microcomputer according to claim 1, wherein the conversion circuit performs a predetermined conversion operation based on a setting by a software.

6. The microcomputer according to claim 1, wherein the nonvolatile memory, the central processing unit, the flag, and the interrupt vector address conversion circuit are integrated on a same semiconductor chip.

7. The microcomputer according to claim 1, wherein

the interrupt program is stored in the first storage area,

the interrupt vector stores a start address of the interrupt program,

the alternate interrupt program that is executed instead of the interrupt program is stored in the second storage area, and

the alternate interrupt vector stores a start address of the alternate interrupt program.

8. The microcomputer according to claim 1, wherein

the interrupt program is stored in the second storage area, and

the interrupt vector and the alternate interrupt vector store a start address of the interrupt program.

9. The microcomputer according to claim 7, wherein a main program is stored in the first storage area.

10. The microcomputer according to claim 8, wherein a main program is stored in the first storage area.

11. The microcomputer according to claim 7, wherein a main program is stored in the second storage area.

12. The microcomputer according to claim 8, wherein a main program is stored in the second storage area.

13. The microcomputer according to claim 7, wherein a main program is stored in a memory other than the nonvolatile memory.

14. The microcomputer according to claim 8, wherein a main program is stored in a memory other than the nonvolatile memory.

15. A microcomputer comprising:

a nonvolatile memory including at least a first storage area and a second storage area in which delete and write of data is electrically performed independently, wherein

a plurality of interrupt vectors indicating respective storage places of a plurality of interrupt programs executed upon requesting of an interrupt is stored in the first storage area, and

a plurality of alternate interrupt vectors corresponding to the respective interrupt vectors is stored in the second storage area;

a central processing unit that has a mechanism to access the nonvolatile memory;

a flag indicating that the first storage area is not accessible; and

a conversion circuit that, based on a state of the flag, performs address conversion so that an area including the interrupt vector accessed by the central processing unit in the first storage area is replaced with an area including the corresponding alternate interrupt vector in the second storage area.

16. The microcomputer according to claim 15, wherein the conversion circuit performs address conversion individually for a plurality of areas including each of the interrupt vectors.

17. The microcomputer according to claim 15, wherein the conversion circuit comprises hardware that performs a predetermined conversion operation.

18. The microcomputer according to claim 15, wherein the conversion circuit performs a predetermined conversion operation based on a setting by a software.

19. The microcomputer according to claim 15, wherein the nonvolatile memory, the central processing unit, the flag, and the interrupt vector address conversion circuit are integrated on a same semiconductor chip.

20. The microcomputer according to claim 15, wherein

the interrupt program is stored in the first storage area,

the interrupt vector stores a start address of the interrupt program,

the alternate interrupt program that is executed instead of the interrupt program is stored in the second storage area, and

the alternate interrupt vector stores a start address of the alternate interrupt program.

21. The microcomputer according to claim 15, wherein

the interrupt program is stored in the second storage area, and

the interrupt vector and the alternate interrupt vector store a

start address of the interrupt program.

22. The microcomputer according to claim 20, wherein a main program is stored in the first storage area.

23. The microcomputer according to claim 21, wherein a main program is stored in the first storage area.

24. The microcomputer according to claim 20, wherein a main program is stored in the second storage area.

25. The microcomputer according to claim 21, wherein a main program is stored in the second storage area.

26. The microcomputer according to claim 20, wherein a main program is stored in a memory other than the nonvolatile memory.

27. The microcomputer according to claim 21, wherein a main program is stored in a memory other than the nonvolatile memory.